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| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/717,103 | YIN, RONG | |
| | Examiner | Art Unit | |
| | Carlos Amaya | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-9 and 15-23* is/are rejected.

7)☒ Claim(s) *4-7,10-14 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: Applicant does not refer to figures 1A, 1B, 2A, 2B, 3A, and 3B; instead applicant refers to figures 1 or 2 or 3. Appropriate correction is required.

### *Claim Objections*

2. Claim1 is objected to because of the following informalities: Examiner does not understand the preferred "normally" state of the switch. The switch should only be referred to as in one of the normally biased states. The claim recites both states "normally open" and "normally closed". Relays are known to have a biased preferred state, either normally open or normally closed not both; and semiconductors witches are controlled based on an applied signal to be in a closed or open state. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. Claims 1,16,21 are rejected under 35 U.S.C. 102(b) as being anticipated by Lopin (US 5,275158).

With respect to claim 1 Lopin discloses a circuit for monitoring the state of at least one switch, comprising: a first circuit (Composed of resistors 124, 126 and MOS transistor 94 Figure 5 for detecting the open and close state of the switches), coupled to

a switch (Switches 116, 118), for detecting whether the switch is in one of a closed state and an open state and generating a signal having a value based upon the detection (Column 7 lines 22-27, See also abstract); and a second circuit (Control circuit 32 Figure 5), coupled to the first circuit, for configuring the first circuit to selectively detect the switch switching from a normally open state and to selectively detect the switch switching from a normally closed state (Control circuit 32 based upon the detection of the switches does a predetermined action).

With respect to claim 16 Lopin discloses method for detecting the state of at least one switch using a circuit, comprising: configuring the circuit to select whether the circuit is to detect a switch switching from a normally open state or from a normally closed state; detecting, by the circuit, the switch switching from the selected state; and generating a signal indicative of the detection. One of ordinary skill in the art would have necessarily performed the recited method steps when using the circuit as disclosed in claim 1.

With respect to claim 21 Lopin discloses 21 a system, comprising: a switch (Switches 116 and 118) having a first conduction terminal and a second conduction terminal (Figure 5 shows the two switches and their respective conductive terminals) a first circuit coupled to the first conduction terminal of the switch the first circuit being configurable to selectively detect the switch being in a closed state and to selectively detect the switch being in an open state. (First circuit is composed of resistors 124, 126 and MOS transistor 94 Figure 5 for detecting the open and close state of the switches).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2-3, 8-9, 15,17-20,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopin (US 5,275158) in view of Youssef (US 6,861,955).

With respect to claim 2 Lopin in view of Youssef discloses the circuit of claim 1. Loping, however, does not disclose expressly that the first circuit includes a third circuit for detecting whether the switch changes from a closed state to an open state and for , pulling a first terminal of the switch to a voltage representative of one of a logic high state and a logic low state.

Youssef discloses in Figure 2 a First circuit 12 (third circuit) for detecting the opening and closing of switch 20 and for pulling terminal 21 of switch 20 to logic low (ground) or logic high (power supply), Column 3 lines 21-23, lines 27-29.

It would have been obvious at the time the invention was made to have combined the Loping circuit for detecting the opening and closing of a switch with Youssef circuit invention for pulling a terminal of the switch to a logic high state and a logic low state.

The suggestion or motivation for doing so would have been to improve the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection of the switch.

With respect to claim 3 Lopin in view of Youssef discloses the circuit of claim 2, wherein the third circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state Youssef (Column 3 lines 21-23, lines 27-29).

With respect to claim 8 Lopin in view of Youssef discloses the circuit of claim 1, wherein the first circuit includes a third circuit for detecting whether the switch changes from an open state to a closed state and for relatively weakly pulling a first terminal of the switch towards a voltage representative of one of a logic high state and a logic low state. As discussed in claim 2 above Youssef discloses a first circuit 12 for detecting the opening and closing of switch 20 and for pulling a terminal to ground or to a power supply. For the purpose of improving the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection state of the switch.

With respect to claim 9 Lopin in view of Youssef discloses the circuit of claim 8, wherein the third circuit is configurable for pulling the first terminal of the switch to a voltage representative of a logic high state and to a logic low state (Column 3 lines 21-23, lines 27-29).

With respect to claim 15 Lopin in view of Youssef discloses the circuit of claim 1, wherein the circuit further comprises: a third circuit for detecting whether a second switch is in one of a closed state and an open state and generating a signal having a value based upon the detection; and a fourth circuit, coupled to the third circuit, for

configuring the third circuit to selectively detect the second switch switching from a normally open state and from a normally closed state. Lopin in view of Youssef discloses the circuit as claimed in claim 3 with the addition of a second switch, Loping discloses Two switches (116 and 118), however Youssef does not disclose a fourth circuit coupled to the third circuit to selectively detect the second switch switching from a normally open state and from a normally closed state. It would have been obvious to one of ordinary skill in the art to have a second switch as disclosed by Lopin and have a fourth circuit to control the second switch in Youssef invention.

The suggestion or motivation for doing so would have been to control/monitor the operation of an apparatus having more than one switch.

With respect to claim 17 and 20 Lopin in view of Youssef discloses the method of claim 16, wherein the step of configuring comprises configuring the circuit to select the circuit detecting the switch switching from the normally closed and normally open state, and to select, during the time the switch is normally closed and normally open, the circuit to relatively weakly pull a terminal of the switch towards a voltage representative of one of a logic high state and a logic low state. One of ordinary skill in the art would have necessarily performed the recited method steps when using the circuit as described in claim 8.

With respect to claim 18 Lopin in view of Youssef discloses the method of claim 17, wherein the step of configuring comprises activating transistors to couple a resistive element between the terminal of the switch and the selected one of the logic high state

and the logic low state. Lopin discloses a transistor 94 couple to a resistor 98 and to a terminal of the switches, however, does not disclose expressly that the activating transistor is couple to a selected one of the logic high stated and low state. Youssef discloses in Figure 2 an activating transistor 16 couple to a resistor 32 between terminal 21 of the switch, transistor 16 by means of first circuit 12 control the switch to connect to a logic high state (Power supply) and a logic low state (ground). It would have been obvious from the teachings of Lopin and Youssef to couple an activating transistor to a resistor between a terminal of the switch and the selected logic high or low state.

The suggestion or motivation for doing so would have been as discussed by Lopin to sense the on or off state of the transistor corresponding to a state of the switches (Column 6 lines 46-48).

With respect to claim 19 Lopin in view of Youssef discloses the method of claim 17, wherein the step of configuring comprises occasionally activating at least one transistor to occasionally couple a resistive element between the terminal of the switch and the selected one of the logic high state and the logic low state. Youssef discloses a pulse generator 18 for controlling transistor 16 couple to resistor 32, Column 3 lines 1-6, 16-19.

With respect to claim 22 Lopin in view of Youssef discloses the system of claim 21. However, Loping does not disclose expressly that the first circuit is configurable to selectively pull the first conduction terminal of the switch towards a voltage level representative of a logic high state, and to selectively pull the first conduction terminal of

the switch towards a voltage level representative of a logic low state. As disclosed by Youssef in claim 2 above, Figure 2 shows a circuit 12 for detecting the opening and closing of switch 20 and for pulling terminal 21 of switch 20 to logic low (ground) or logic high (power supply), Column 3 lines 21-23, lines 27-29. For the purpose of improving the reliability and operability of the switch and to make sure the switch and the circuits are giving the right output based on the detection of the switch.

With respect to claim 23 Lopin in view of Youssef discloses the system of claim 22, wherein the first circuit selectively weakly pulls the first terminal of the switch towards a pre-selected logic state, relative to a drive strength of the switch to pull the first terminal thereof towards a different logic state. Youssef (Column 3 lines 12-15, 21-23 and lines 27-29).

***Allowable Subject Matter***

7. Claims 4-7, 10-14, 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 4 is allowable over the prior art of record, because the prior art of record does not suggests that "a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source; a second transistor coupled between the first terminal of the at least one resistive element and the first terminal of the switch; a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source, and a fourth transistor coupled

between the second terminal of the at least one resistive element and the first terminal of the switch".

9. Claims 5-7 are allowable because they depend on allowable claims.

10. Claim 10 is allowable over the prior art of record, because the prior art of record does not suggests that "the third circuit comprises at least one first transistor coupled between a high reference voltage level and the first terminal of the switch, at least one second transistor coupled between a low reference voltage level and the first terminal of the switch, and control logic for generating at least one control signal having a value indicative of a configuration of the third circuit, a control terminal of each of the at least one first transistor and the at least one second transistor having a value based upon the value of the at least one control signal".

11. Claims 11-14 are allowable because they depend on allowable claims.

12. Claim 24 is allowable over the prior art of record, because the prior art of record does not suggests that "a first transistor coupled between a first terminal of the at least one resistive element and a high reference voltage source; a second transistor coupled between the first terminal of the at least one resistive element and the first conduction terminal of the switch; a third transistor coupled between a second terminal of the at least one resistive element and a low reference voltage source; and a fourth transistor coupled between the first conduction terminal of the switch and the second terminal of the at least one resistive element".

13. Claims 25-26 are allowable because they depend on allowable claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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